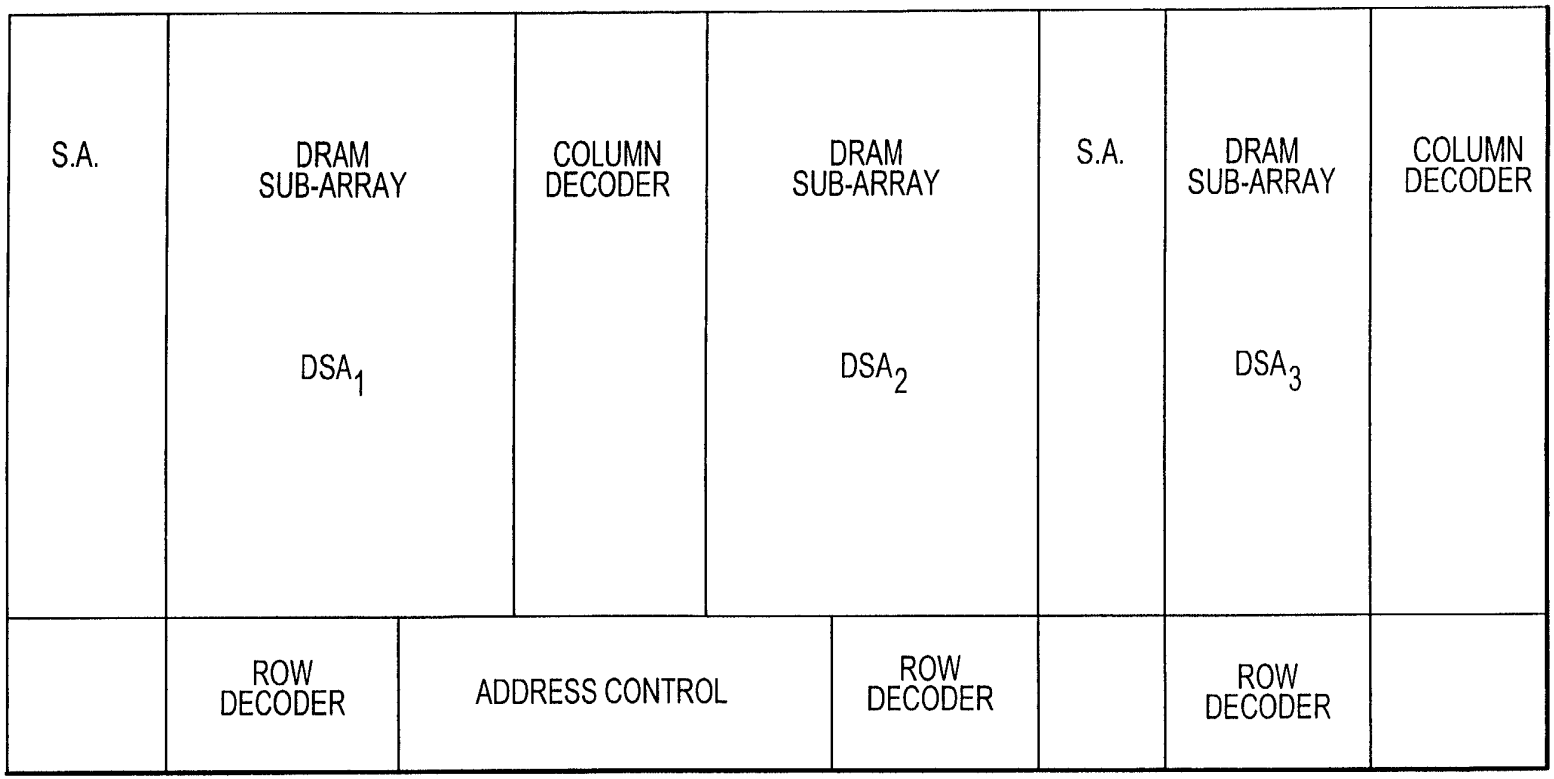
S.A.
DRAM SUB-ARRAY
DSA1
COLUMN DECODER
DRAM SUB-ARRAY
DSA2
S.A.
DRAM SUB-ARRAY
DSA3
COLUMN DECODER
ROW DECODER
ADDRESS CONTROL
ROW DECODER
ROW DECODER

FIG.1A

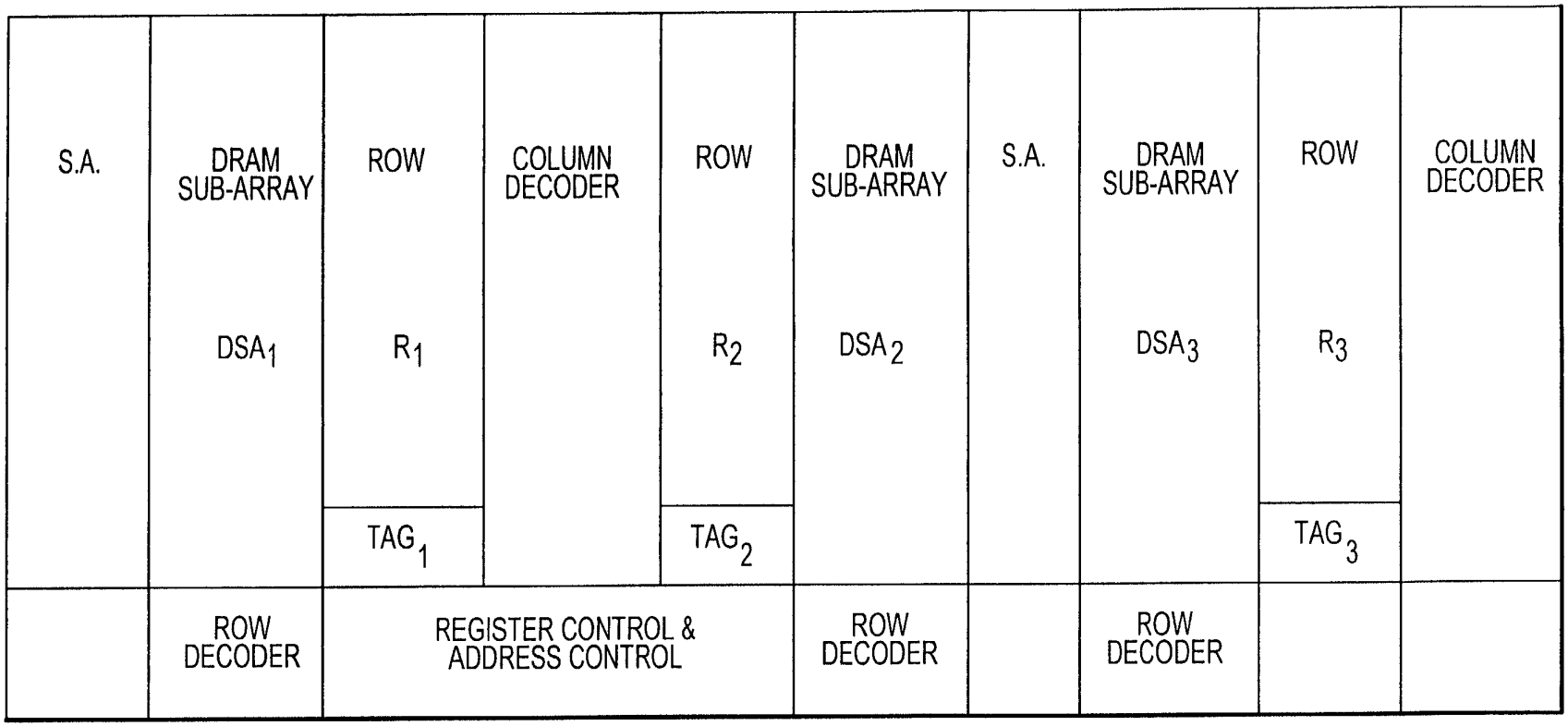
S.A.
DRAM SUB-ARRAY
DSA1
ROW
R1
TAG1
COLUMN DECODER
ROW
R2
TAG2
DRAM SUB-ARRAY
DSA2
S.A.
DRAM SUB-ARRAY
DSA3
ROW
R3
TAG3
COLUMN DECODER
ROW DECODER
REGISTER CONTROL & ADDRESS CONTROL
ROW DECODER
ROW DECODER

FIG.1B

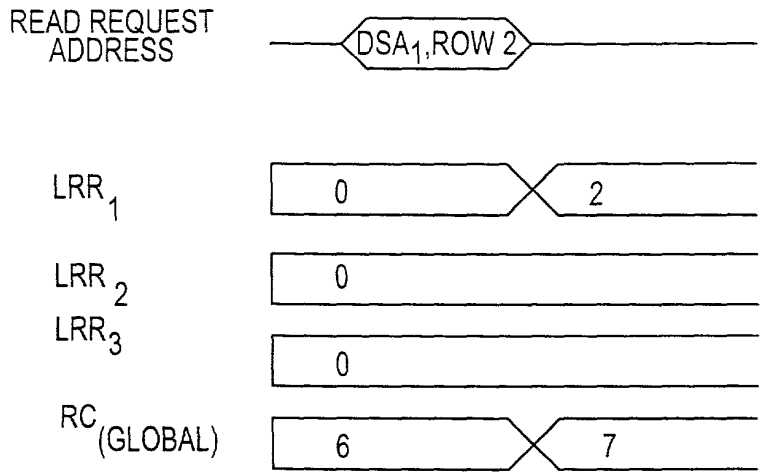

FIG.2

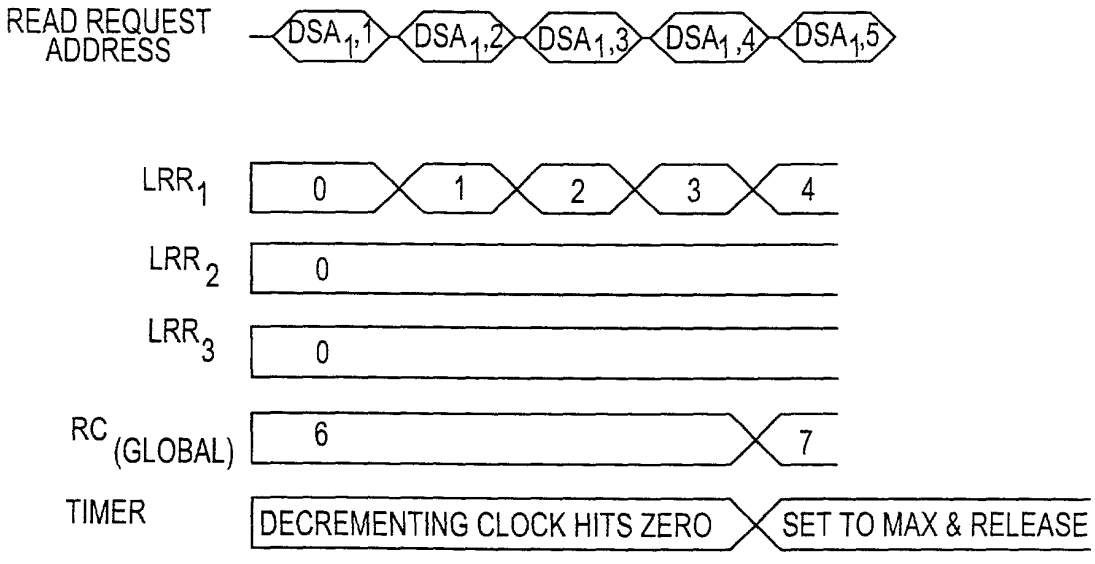

FIG.3

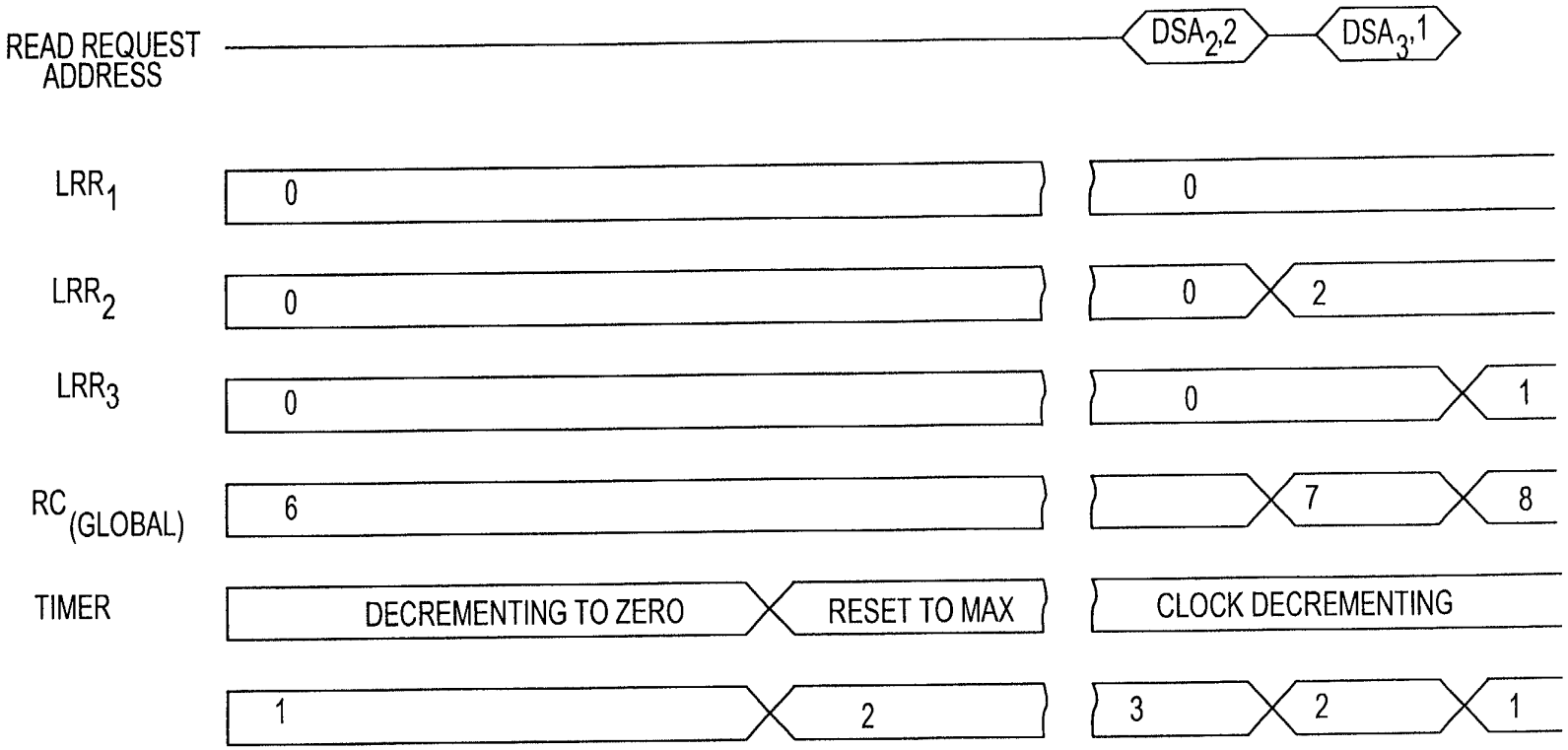
READ REQUEST ADDRESS
DSA2,2
DSA3,1
LRR1
LRR2
LRR3
RC (GLOBAL)
TIMER
0
0
0
0
0
2
0
1
6
7
8
DECREMENTING TO ZERO
RESET TO MAX
CLOCK DECREMENTING
1
2
3
2
1

FIG.4

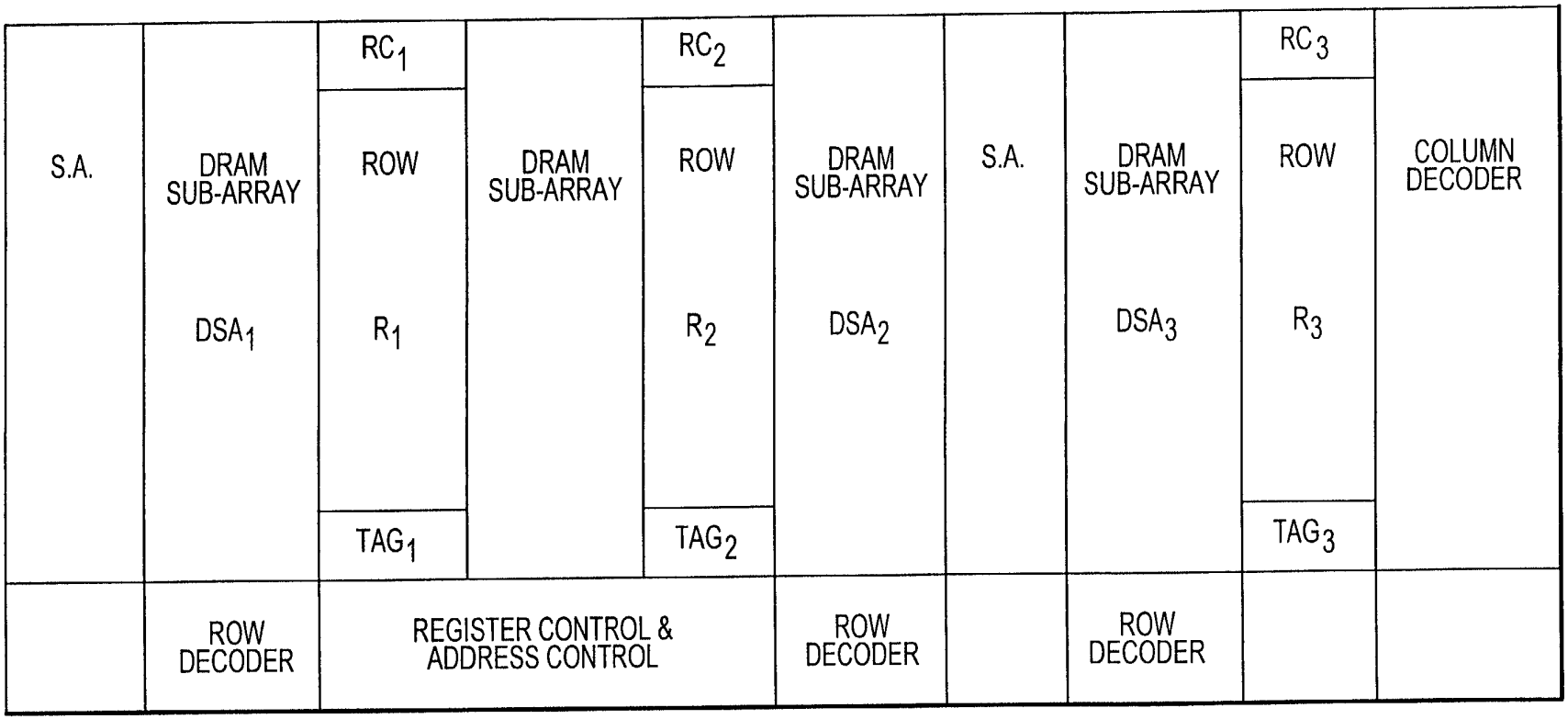
S.A.
DRAM SUB-ARRAY
DSA1
RC1
ROW
R1
TAG1
DRAM SUB-ARRAY
RC2
ROW
R2
TAG2
DRAM SUB-ARRAY
DSA2
S.A.
DRAM SUB-ARRAY
DSA3
RC3
ROW
R3
TAG3
COLUMN DECODER
ROW DECODER
REGISTER CONTROL & ADDRESS CONTROL
ROW DECODER
ROW DECODER

FIG.5

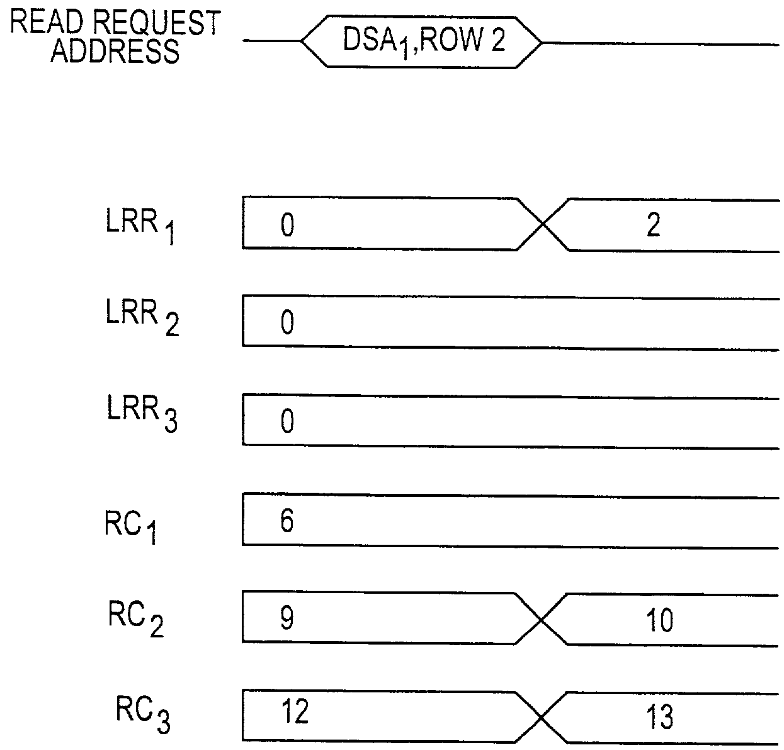
READ REQUEST ADDRESS
DSA1,ROW 2
LRR 1
0
2
LRR 2
0
LRR 3
0
RC1
6
RC2
9
10
RC3
12
13

FIG.6

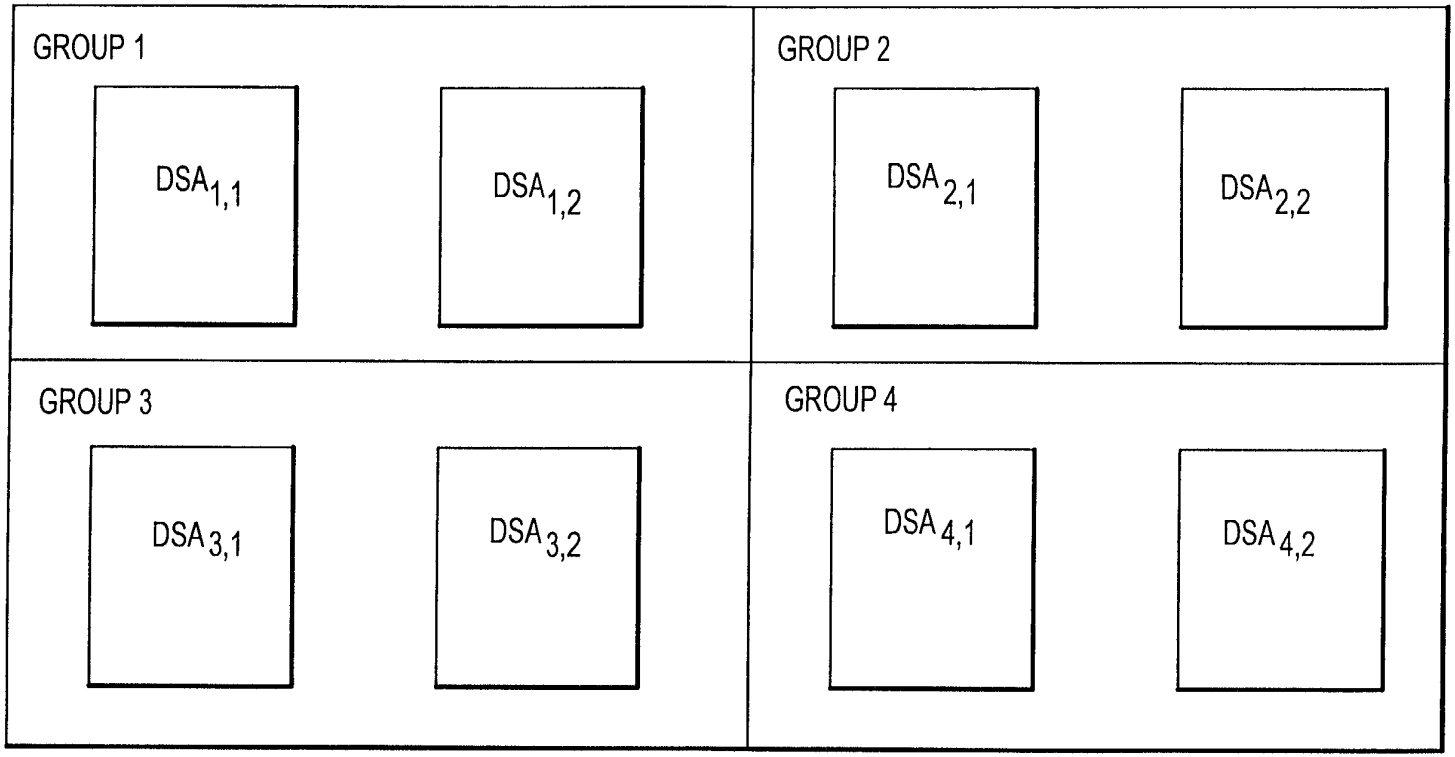
GROUP 1
DSA1,1
DSA1,2
GROUP 2
DSA2,1
DSA2,2
GROUP 3
DSA3,1
DSA3,2
GROUP 4
DSA4,1
DSA4,2

FIG.7

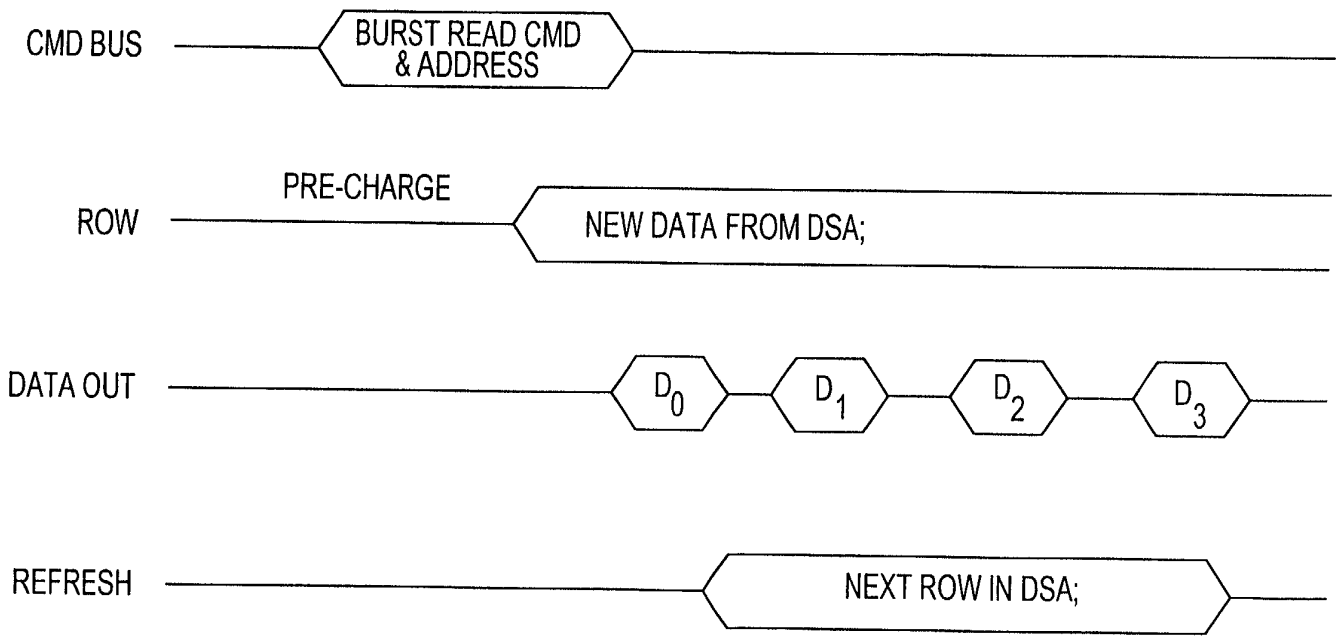
CMD BUS
BURST READ CMD & ADDRESS
ROW
PRE-CHARGE
NEW DATA FROM DSA;
DATA OUT
D0
D1
D2
D3
REFRESH
NEXT ROW IN DSA;

FIG.8